AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

Claim 1 (canceled).

2. (currently amended) The method of claim [[1]] 3, wherein said pair of microstrips has a width that increases as it is outwardly routed.

3. (currently amended) A method comprising:

providing a substrate;

forming a plurality of microstrips on said substrate,

at least a pair of said plurality of microstrips for transmitting signals,

said pair of said plurality of microstrips ("said pair of microstrips") for being capacitively coupled to each other, through a first length,

said pair of microstrips for having substantially constant characteristic impedance throughout substantially the entire length of said pair of microstrips,

~~The method of claim 1,~~ wherein a width of each of said pair of microstrips along said first ~~partial~~ length is less than a width determined from an equation 50 ohm = 1 / vC, where v is a velocity of propagation of the signals and C is a capacitance per unit length.

4. (currently amended) The method of claim [[1]] 3, wherein said substrate is made of substantially Alumina.

5. (currently amended) The method of claim [[1]] 3, further comprising: ~~wherein said IC is~~

connecting a demultiplexor or multiplexor chip for OC-768 applications to said substrate.

6. (currently amended) The method of claim [[1]] 3, wherein said signals comprise high-speed data signals operating at a ~~frequency~~ rate of at least 20 Gbps.

7. (currently amended) The method of claim [[1]] 3, further comprising: ~~wherein said external terminals comprise~~

coupling a pair of coaxial terminals to said pair of microstrips.

8. (currently amended) The method of claim [[1]] 3, wherein said first ~~partial~~ length is located substantially at a first end of said pair of microstrips,

wherein said first end is located near an inner edge of said substrate for receiving said signals from ~~said~~ an integrated circuit ("IC").

9. (currently amended) A method comprising:

providing a substrate;

forming a plurality of microstrips on said substrate,

at least a pair of said plurality of microstrips for transmitting signals,

said pair of said plurality of microstrips ("said pair of microstrips") for being capacitively coupled to each other, through a first length,

said pair of microstrips for having substantially constant characteristic impedance throughout substantially the entire length of said pair of microstrips,

~~The method of claim 1,~~ wherein along a second ~~partial~~ length within said first ~~partial~~ length of said pair of microstrips, said pair of microstrips is widened to increase its capacitance.

10. (currently amended) The method of claim 9, wherein said second ~~partial~~ length is located substantially at a first end of said pair of microstrips,

wherein said first end is located near an inner edge of said substrate for receiving said signals from ~~said~~ an integrated circuit ("IC").

11. (currently amended) A method comprising:

providing a substrate;

forming a plurality of microstrips on said substrate,

at least a pair of said plurality of microstrips for transmitting signals,

said pair of said plurality of microstrips ("said pair of microstrips") for being capacitively coupled to each other, through a first length,

said pair of microstrips for having substantially constant characteristic impedance throughout substantially the entire length of said pair of microstrips,

coupling a pair of coaxial terminals to said pair of microstrips,

~~The method of claim 7,~~ wherein along a second ~~partial~~ length within said first ~~partial~~ length of said pair of microstrips, said pair of microstrips is widened to increase its capacitance.

12. (currently amended) The method of claim [[1]] 3, wherein a width of each of said pair of microstrips along a portion of said first ~~partial~~ length is not more than 5 mils,

wherein spacing between said pair of microstrips along a portion of said first ~~partial~~ length is not more than 5 mils.

13. (currently amended) The method of claim [[1]] 3, wherein said pair of microstrips is substantially 50-ohm transmission lines throughout substantially the entire length of said pair of microstrips.

14. (currently amended) The method of claim [[1]] 3, wherein said signals are differential signals.

15. (currently amended) The method of claim [[1]] 3, wherein said substrate is a single-layer substrate.

16. (currently amended) The method of claim [[1]] 3, wherein said substrate is a multiple-layer substrate.

17. (original) The method of claim 7, wherein a width of a dielectric ring portion of one of said pair of coaxial terminals is substantially identical to a thickness of said substrate.

18. (currently amended) The method of claim [[1]] 3, further comprising: ~~wherein said external terminals comprise~~

coupling GPPO connectors to said pair of microstrips.

Claim 19 (canceled).

20. (currently amended) The method of claim [[1]] 3, wherein said pair of microstrips are for transmitting high-speed signals,

wherein said plurality of microstrips further comprise a second plurality of microstrips that are for transmitting low speed signals.

21. (currently amended) A method for forming a package for ~~connecting~~ at least one ~~high speed~~ integrated circuit chip ("IC"), said IC for comprising at least one high speed signal and low speed signals, said method comprising:

providing a substrate ~~to mount~~ for mounting said IC;

forming at least one external coaxial connector for communicating said [[high-speed]] high speed signal,

forming ~~an array~~ a plurality of terminals ~~at a bottom side of~~ on said substrate for communicating at least said low speed signals;

~~selectively~~ forming a plurality of first microstrips on ~~a top surface of~~ said substrate,

at least one of said plurality of first microstrips being disposed for connecting said high speed signal between said IC and said at least one external coaxial connector,

at least another one of said plurality of first microstrips being disposed for connecting one of said low speed signals between said IC and one of said plurality ~~array~~ of terminals;

~~selectively~~ forming a plurality of interconnections within said substrate,

wherein at least one of said plurality of interconnections connects at least said at least another one of said plurality of first microstrips to at least said one ~~terminal~~ of said plurality ~~array~~ of terminals,

wherein said at least one of said plurality of first microstrips and said at least one external coaxial connector are for providing substantially constant characteristic impedance throughout substantially said at least one of said plurality of first microstrips and said at least one external coaxial connector.

wherein said substrate comprises a plurality of dielectric layers formed by a low-temperature co-fired ceramics process, not a printed circuit board.

22. (currently amended) The method of claim [21] 30, wherein a rate of said high speed signal is at least 20 Gbps, and a rate of one of said low speed signals is lower than 20 Gbps.

23. (currently amended) The method of claim [21] 30, wherein said at least another one of said plurality of first microstrips is for providing substantially constant characteristic impedance,

wherein at least one of said plurality of interconnections is for providing substantially constant characteristic impedance throughout said at least one of said plurality of interconnections connecting at least said at least another one of said plurality of first microstrips to at least said one ~~terminal~~ of said plurality ~~array~~ of terminals.

24. (currently amended) The method of claim [21] 30, wherein said at least one external coaxial connector is placed on a side of said substrate.

25. (currently amended) The method of claim [21] 30, said [[high-speed]] high speed signal does not transmit through said substrate.

26. (currently amended) The method of claim [21] 30, wherein said at least one external coaxial connector comprises a GPPO connector.

27. (currently amended) The method of claim [21] 30, wherein said plurality ~~array~~ of terminals comprises ball grid array ("BGA") terminals.

28. (currently amended) The method of claim [21] 30, wherein said substrate comprises at least a first dielectric layer and a second dielectric layer.

Claim 29 (canceled).

30. (currently amended) A method for forming a package for at least one integrated circuit ("IC"), said IC for carrying at least one high speed signal and low speed signals, said method comprising:

providing a substrate for mounting said IC;

forming at least one external coaxial connector for communicating said high speed signal,

forming a plurality of terminals on said substrate for communicating at least said low speed signals;

forming a plurality of first microstrips on said substrate,

at least one of said plurality of first microstrips being disposed for connecting said high speed signal between said IC and said at least one external coaxial connector,

at least another one of said plurality of first microstrips being disposed for connecting one of said low speed signals between said IC and one of said plurality of terminals;

forming a plurality of interconnections within said substrate,

wherein at least one of said plurality of interconnections connects at least said at least another one of said plurality of first microstrips to at least said one of said plurality of terminals,

wherein said at least one of said plurality of first microstrips and said at least one external coaxial connector are for providing substantially constant characteristic impedance throughout substantially said at least one of said plurality of first microstrips and said at least one external coaxial connector,

~~The method of claim 21,~~ wherein said substrate comprises a plurality of dielectric layers formed by a high-temperature co-fired ceramics process.

Claims 31, 32 and 33 (canceled).

34. (currently amended) ~~The method of claim 33, further comprising:~~

A method for forming a package for at least one integrated circuit ("IC"), said IC for carrying at least one high speed signal and low speed signals, said method comprising:

providing a substrate for mounting said IC;

forming at least one external coaxial connector for communicating said high speed signal,

forming a plurality of terminals on said substrate for communicating at least said low speed signals;

forming a plurality of first microstrips on said substrate,

at least one of said plurality of first microstrips being disposed for connecting said high speed signal between said IC and said at least one external coaxial connector,

at least another one of said plurality of first microstrips being disposed for connecting one of said low speed signals between said IC and one of said plurality of terminals;

forming a plurality of interconnections within said substrate,

wherein at least one of said plurality of interconnections connects at least said at least another one of said plurality of first microstrips to at least said one of said plurality of terminals,

wherein said at least one of said plurality of first microstrips and said at least one external coaxial connector are for providing substantially constant characteristic impedance throughout substantially said at least one of said plurality of first microstrips and said at least one external coaxial connector,

wherein said step of forming a plurality of first microstrips comprises:

forming at least a ground path for said at least one of said plurality of first microstrips ("high-speed microstrip");

widening said high-speed microstrip through a second ~~partial~~ length to increase its capacitance,[[.]]

wherein said ground path is for being capacitively coupled to said high-speed microstrip through a first length.

35. (currently amended) The method of claim [21] 30,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein [[said]] a top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of ~~selectively~~ forming a plurality of interconnections comprises:

~~selectively~~ forming a plurality of second paths between said first and second dielectric layers;

~~selectively~~ forming a plurality of third paths at a bottom of said second dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of third paths through a via connection;

wherein said via connection is underneath said at least one of said plurality of first microstrips;

wherein said at least one of said plurality of second paths and said at least one of said plurality of third paths form a continuous ground path.

36. (original) The method of claim 35,

wherein said at least one of said plurality of second paths is for providing substantially constant characteristic impedance along said at least one of said plurality of second paths;

wherein said via connection is for providing substantially constant characteristic impedance along said via connection;

wherein said at least one of said plurality of third paths is for providing substantially constant characteristic impedance along said at least one of said plurality of third paths.

37. (original) The method of claim 35, further comprising:

tapering out said at least one of said plurality of first microstrips at a tapering section,

wherein said via connection is underneath said tapering section.

38. (currently amended) The method of claim [21] 30,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein [[said]] a top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of ~~selectively~~ forming a plurality of interconnections comprises:

~~selectively~~ forming a plurality of second transmission lines between said first and second dielectric layers;

~~selectively~~ forming a plurality of third transmission lines at a bottom of said second dielectric layer,

~~selectively~~ forming a plurality of first via connections in said first dielectric layer, and

~~selectively~~ forming a plurality of second via connections in said second dielectric layer,

wherein one of said plurality of first via connections connects said at least another one of said plurality of first microstrips to one of said plurality of second transmission lines,

wherein one of said plurality of second via connections connects said one of said plurality of second transmission lines to one of said plurality of third transmission lines,

wherein said one of said plurality of first via connections is aligned with said one of said plurality of second via connections.

39. (currently amended) The method of claim [21] 30,

wherein said at least one of said plurality of first microstrips comprises a first ~~partial~~ length near an inner edge of said substrate and a second ~~partial~~ length toward an outer edge of said substrate,

wherein a width along said second ~~partial~~ length is wider than a width along a portion of said first ~~partial~~ length.

40. (currently amended) The method of claim 39,

wherein said first ~~partial~~ length comprises a third ~~partial~~ length and a fourth ~~partial~~ length,

wherein said third ~~partial~~ length is closer to said inner edge than said fourth ~~partial~~ length is to said inner edge,

wherein a width along said third ~~partial~~ length is wider than a width along said fourth ~~partial~~ length.

41. (currently amended) The method of claim [21] 30,

wherein said substrate comprises at least a first dielectric layer, a second dielectric layer, and a third dielectric layer

wherein [[said]] a top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of ~~selectively~~ forming a plurality of interconnections comprises:

~~selectively~~ forming a plurality of second paths between said first and second dielectric layers;

~~selectively~~ forming a plurality of third paths between said second and third dielectric layers;

~~selectively~~ forming a plurality of fourth paths at a bottom of said third dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of fourth paths through at least a first via connection and a second via connection;

wherein said at least another one of said plurality of first microstrips is connected to one of said plurality of third paths,

wherein spacing between said first via connection and said second via connection is less than a wavelength of the highest frequency signal that is to be carried along said one of said plurality of third paths.

42. (original) The method of claim 41,

wherein spacing between said first via connection and said one of said plurality of third paths is about half of a separation between said at least one of said plurality of second paths and a said at least one of said plurality of fourth paths.

43. (currently amended) The method of claim [21] 30, wherein said substrate is less than 0.4 cubic inches.

44. (currently amended) The method of claim [21] 30,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein [[said]] a top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of ~~selectively~~ forming a plurality of interconnections comprises:

~~selectively~~ forming a plurality of second paths between said first and second dielectric layers;

~~selectively~~ forming a plurality of third paths at a bottom of said second dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of third paths through a via connection;

wherein a first portion of said at least one of said plurality of first microstrips is over a portion of said at least one of said plurality of second paths,

wherein a second portion of said at least one of said plurality of first microstrips is over said via connection,

wherein a third portion of said at least one of said plurality of first microstrips is over a portion of said at least one of said plurality of third paths,

wherein said first portion is narrower than said third portion,

wherein said second portion tapers out from said first portion toward said third portion,

wherein said first portion, said second portion and said third portion are for providing substantially constant impedance along said first portion, said second portion and said third portion.

45. (currently amended) A method for forming a package for at least one integrated circuit ("IC"), said IC for carrying at least one high speed signal and low speed signals, said method comprising:

providing a substrate for mounting said IC;

forming at least one external coaxial connector for communicating said high speed signal,

forming a plurality of terminals on said substrate for communicating at least said low speed signals;

forming a plurality of first microstrips on said substrate,

at least one of said plurality of first microstrips being disposed for connecting said high speed signal between said IC and said at least one external coaxial connector,

at least another one of said plurality of first microstrips being disposed for connecting one of said low speed signals between said IC and one of said plurality of terminals;

forming a plurality of interconnections within said substrate,

wherein at least one of said plurality of interconnections connects at least said at least another one of said plurality of first microstrips to at least said one of said plurality of terminals,

wherein said at least one of said plurality of first microstrips and said at least one external coaxial connector are for providing substantially constant characteristic impedance throughout substantially said at least one of said plurality of first microstrips and said at least one external coaxial connector,

wherein one of said plurality of interconnections comprises a via connection,

wherein said via connection comprises a conductor core for a signal,

wherein said conductor core is surrounded by a dielectric material portion of said substrate and bound by a circular opening for a ground signal,

~~The method of claim 32,~~

wherein said via connection's impedance is determined substantially by:

$$60 \log (b/a) / [\eta \times \varepsilon] \; [\eta \times \sqrt{\varepsilon}]$$

wherein b is a diameter of said circular opening, a is a diameter of said conductor core, ε is a dielectric constant of said dielectric material portion, and η is an efficiency of a capacitance between said circular opening and said conductor core as compared to that in a coaxial cable having same a and b dimensions.

Claim 46 (canceled).

47. (currently amended)

A method for making a package for connecting at least one integrated circuit ("IC") to a plurality of terminals, comprising:

providing a substrate comprising a plurality of dielectric layers;

forming a plurality of microstrips on said substrate, at least one of said plurality of microstrips ("high-speed microstrip") being disposed for conducting a high speed signal between said IC and one of said plurality of terminals;

forming at least a first ground path near said high-speed microstrip, said first ground path for being capacitively coupled to said high-speed microstrip at least through a first length of said high-speed microstrip;

forming a second ground path at a first vertical distance below said high-speed microstrip in said substrate;

forming a third ground path at a second vertical distance below said high-speed microstrip in said substrate;

forming at least one via connector to connect said second and third ground paths;

forming a plurality of internal striplines in said substrate, said plurality of internal striplines for connecting signals between said IC and a second set of terminals;

forming a plurality of internal coaxial connectors in said substrate, being adapted for connecting said plurality of internal striplines through said substrate;

~~The method of claim 46, further comprising:~~

widening said high-speed microstrip through a second ~~partial~~ length while maintaining its capacitance.

48. (currently amended) The method of claim [[46]] 47, further comprising:

forming said at least one via connector below said high-speed microstrip.

49. (currently amended) The method of claim [[46]] 47, wherein said one of said plurality of ~~external~~ terminals connected to said high-speed microstrip is a coaxial GPPO connector.

50. (currently amended) The method of claim [[46]] 47, wherein said second set of ~~external~~ terminals are BGA connectors.

51. (currently amended) The method of claim [[46]] 47, wherein said high-speed microstrip is capable of carrying a signal at a rate of at least 30 Gbps.

52. (currently amended) The method of claim [[46]] 47, further comprising:

forming at least a pair of said plurality of microstrips to connect a pair of high-speed differential signals.

Claim 53 (canceled).

54. (currently amended) ~~The method of claim 53,~~

A method for forming a package for an integrated circuit ("IC"), said method comprising:

providing a substrate comprising a plurality of dielectric layers;

providing a plurality of coaxial connectors;

providing a plurality of BGA connectors;

forming a plurality of microstrips on a first layer of said plurality of dielectric layers, being disposed for connecting to said IC,

some of said plurality of microstrips ("first microstrips") coupled to said plurality of coaxial connectors;

forming a plurality of internal connections on a second layer of said plurality of dielectric layers;

forming a plurality of inter-layer connections in said substrate,

said plurality of inter-layer connections coupling some of said plurality of microstrips ("second microstrips") to said plurality of internal connections and coupling said plurality of internal connections to said plurality of BGA connectors,

wherein said plurality of microstrips comprise a pair of microstrips for high speed differential signals and ~~three co-planar~~ a plurality of ground paths ~~strips~~, said pair of microstrips for high speed differential signals for being capacitively coupled to said ~~three co-planar~~ plurality of ground paths ~~strips~~ through a first ~~partial~~ length;

wherein said pair of microstrips for high speed differential signals are widened in width from an inner edge of said substrate to an outer edge of said substrate, said pair of microstrips for high speed differential signals for maintaining their capacitance substantially constant.

55. (currently amended) The method of claim [53] 54,

wherein said step of ~~selectively~~ forming a plurality of internal connections comprises:

forming internal striplines to connect active signals; and

forming ground strips to connect to ground;

wherein said step of ~~selectively~~ forming a plurality of inter-layer connections comprises:

forming internal coaxial conductors to connect active signals;

forming via connectors to connect to ground.

56. (currently amended) The method of claim [53] 54, a path throughout substantially said first microstrips and said plurality of coaxial connectors ~~terminals~~ for providing substantially constant impedance,

wherein a rate of said ~~first signals~~ high speed differential signals is at least 20 Gbps.

Claims 57-59 (canceled).

60. (new) The method of claim 21, wherein a rate of said high speed signal is at least 20 Gbps, and a rate of one of said low speed signals is lower than 20 Gbps.

61. (new) The method of claim 21, wherein said plurality of terminals comprises ball grid array ("BGA") connectors.

62. (new) The method of claim 21,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein a top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of forming a plurality of interconnections comprises:

forming a plurality of second paths between said first and second dielectric layers;

forming a plurality of third paths at a bottom of said second dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of third paths through a via connection;

wherein said via connection is underneath said at least one of said plurality of first microstrips;

wherein said at least one of said plurality of second paths and said at least one of said plurality of third paths form a continuous ground path.

63. (new) The method of claim 21,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein a top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of forming a plurality of interconnections comprises:

forming a plurality of second transmission lines between said first and second dielectric layers;

forming a plurality of third transmission lines at a bottom of said second dielectric layer,

forming a plurality of first via connections in said first dielectric layer, and

forming a plurality of second via connections in said second dielectric layer,

wherein one of said plurality of first via connections connects said at least another one of said plurality of first microstrips to one of said plurality of second transmission lines,

wherein one of said plurality of second via connections connects said one of said plurality of second transmission lines to one of said plurality of third transmission lines,

wherein said one of said plurality of first via connections is aligned with said one of said plurality of second via connections.

64. (new) The method of claim 21,

wherein said substrate comprises at least a first dielectric layer, a second dielectric layer, and a third dielectric layer

wherein a top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of forming a plurality of interconnections comprises:

forming a plurality of second paths between said first and second dielectric layers;

forming a plurality of third paths between said second and third dielectric layers;

forming a plurality of fourth paths at a bottom of said third dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of fourth paths through at least a first via connection and a second via connection;

wherein said at least another one of said plurality of first microstrips is connected to one of said plurality of third paths,

wherein spacing between said first via connection and said second via connection is less than a wavelength of the highest frequency signal that is to be carried along said one of said plurality of third paths.

65. (new) The method of claim 21,

wherein said substrate comprises at least a first dielectric layer and a second dielectric layer,

wherein a top surface of said substrate is a top surface of said first dielectric layer,

wherein said step of forming a plurality of interconnections comprises:

forming a plurality of second paths between said first and second dielectric layers;

forming a plurality of third paths at a bottom of said second dielectric layer,

wherein at least one of said plurality of second paths is for a ground signal and connected to at least one of said plurality of third paths through a via connection;

wherein a first portion of said at least one of said plurality of first microstrips is over a portion of said at least one of said plurality of second paths,

wherein a second portion of said at least one of said plurality of first microstrips is over said via connection,

wherein a third portion of said at least one of said plurality of first microstrips is over a portion of said at least one of said plurality of third paths,

wherein said first portion is narrower than said third portion,

wherein said second portion tapers out from said first portion toward said third portion,

wherein said first portion, said second portion and said third portion are for providing substantially constant impedance along said first portion, said second portion and said third portion.

66. (new) The method of claim 47, wherein said one of said plurality of terminals is a coaxial connector,

wherein said second set of terminals are BGA connectors,

wherein said high-speed microstrip is for carrying a differential signal,

wherein said high-speed microstrip is for having substantially constant characteristic impedance throughout substantially the entire length of said high-speed microstrip,

wherein said high-speed microstrip is for carrying a signal at a rate of at least 30 Gbps,

wherein said capacitance is a capacitance to ground.

67. (new) The method of claim 54, wherein said plurality of ground paths comprise three co-planar ground strips.